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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte MICHAEL N. DERR

Appeal 2008-005419
Application 09/821,116
Technology Center 2400

Decided: August 7, 2009

Before HOWARD B. BLANKENSHIP, JEAN R. HOMERE, and JAY P. LUCAS, *Administrative Patent Judges*.

BLANKENSHIP, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

This is an appeal under 35 U.S.C. § 134(a) from the Examiner's final rejection of claims 2, 3, and 5-25, which are all of the pending claims in this application. We have jurisdiction under 35 U.S.C. § 6(b).

We affirm the Examiner's rejection of claims 2, 3, 5-14, and 16-25. We reverse, *pro forma*, the Examiner's rejection of claim 15, and enter a new ground of rejection against the claim.

Invention

Appellant's invention relates to a method, computer, and software program for bit-granular writes of control registers. The method receives data of a single write command wherein the data comprises a bit enable field 401 and a data field 402 comprising N bits in each field (Fig. 4; Spec. 13:9-19). A register is updated with one or more bits of the data field that are associated with enabled bits of the bit enable field (*id.*).

Representative Claim

20. A method comprising

receiving data of a single write command wherein the data comprises a bit enable field and a data field comprising N bits in each field, and

updating a register with one or more bits of the data field that are associated with enabled bits of the bit enable field.

Prior Art

Baker	5,996,032	Nov. 30, 1999
Runaldue	5,999,441	Dec. 7, 1999

Examiner's Rejections

Claims 2, 3, and 5-25 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Baker and Runaldue.

Claim Groupings

Based on Appellant's arguments in the Appeal Brief, we will decide the appeal on the basis of claims 6-8, 10, 12, 15, 16, 20, and 22. *See* 37 C.F.R. § 41.37(c)(1)(vii).

ISSUES

The principal issues on appeal are:

(1) Has Appellant shown that the Examiner erroneously concluded that the combination of Baker and Runaldue teaches receiving data of a single write command, the data comprising a bit enable field and a data field that comprise N bits in each field, and updating a register with one or more bits of the data field that are associated with enabled bits of the bit enable field; and

(2) Does claim 15 meet the requirements of 35 U.S.C. § 112, second paragraph?

FINDINGS OF FACT

1. Baker teaches a system for writing a plurality of data bits less than the total number of bits in a data register using a single register write operation (Title, Abstract).

2. Fig. 10 shows register write circuitry 250 for writing an arbitrary number of data register bits with a single register write operation. Circuitry 250 shows one of an arbitrary number of similar circuits, each circuit controlling a particular bit out of the arbitrary number of data bits. Fig. 10; col. 16, ll. 31-36.

3. Register write circuitry 250 permits writing only to bits that are to be changed in a register, while preserving the previous value of the remainder of bits (col. 16, ll. 47-49).

4. When there is an address of a register to which the write enable bit 258 is set, 1 to 4 GPIOs (general purpose I/O's) may be written to, based on the address field. The A_x's in [GPIO] address number input 266 represent the respective address bit. The write strobe 264 indicates a write operation. The GPIO Address OK 262 is a basic address decode for the entire register. Col. 16, ll. 53-60.

5. The write enable 258 to flip-flop 254 is the AND function output (col. 16, ll. 60-61).

6. When the write enable is active, input write data 252 is written to flip-flop 254 and appears on flip-flop output 270. Col. 16, ll. 61-63.

7. Fig. 11 shows address field 272 that includes GPIO register address bits 274 and individual bit select field 276 address bits A_0, A_1, A_2, and A_3 according to the bit value, 0 or 1, of the associated bits in address field 272. The latter two bits 278 of address field 272 generally assume a zero value. In address 272, the two least significant bits assume a zero value due to the bus architecture. The next four bits specified as A_0, A_1, A_2, and A_3 permit addressing four bits individually or in different combinations.

The higher order or most significant bits are the particular addresses specified or allocated for this particular function. Therefore, a fixed set of bit patterns address the given GPIO address value to select the particular addresses. The result is an entire array of addresses from 0000 to 1111 (i.e., 16 different possible combinations) that could be addressed. Col. 16, l. 64 to col. 17, l. 11.

PRINCIPLES OF LAW

Claim Interpretation

During examination, claims are to be given their broadest reasonable interpretation consistent with the specification, and the language should be read in light of the specification as it would be interpreted by one of ordinary skill in the art. *In re Amer. Acad. of Sci. Tech Ctr.*, 367 F.3d 1359, 1364 (Fed. Cir. 2004) (citations omitted). The Office must apply the broadest reasonable meaning to the claim language, taking into account any definitions presented in the specification. *Id.* (citing *In re Bass*, 314 F.3d 575, 577 (Fed. Cir. 2002)).

Obviousness

The question of obviousness is resolved on the basis of underlying factual determinations including (1) the scope and content of the prior art, (2) any differences between the claimed subject matter and the prior art, and (3) the level of skill in the art. *Graham v. John Deere Co.*, 383 U.S. 1, 17 (1966). "The combination of familiar elements according to known methods

is likely to be obvious when it does no more than yield predictable results." *KSR Int'l Co. v. Teleflex, Inc.*, 550 U.S. 398, 416 (2007).

Indefiniteness

A prior art rejection cannot be sustained if the hypothetical person of ordinary skill in the art would have to make speculative assumptions concerning the meaning of claim language. *In re Steele*, 305 F.2d 859, 862 (CCPA 1962). *See also In re Wilson*, 424 F.2d 1382, 1385 (CCPA 1970) ("If no reasonably definite meaning can be ascribed to certain terms in the claim, the subject matter does not become obvious-the claim becomes indefinite.").

ANALYSIS

Claim 20

Appellant contends that Baker does not teach receiving data of a write command wherein the data comprises a bit enable field and a data field comprising the same number of bits and then updating a register with one or more bits of the data field that are associated with enable bits of the bit enable bits (App. Br. 6-7; Reply Br. 11). Appellant further contends that the combination of Baker and Runaldue does not teach the receiving and updating steps of claim 20 (App. Br. 8).

The Examiner finds that Baker teaches receiving data of a write command comprising a bit enable field and a data field, wherein the bit enable field and the data field comprises the same number of bits in each field (Ans. 8-11). We agree with the Examiner.

Baker teaches a system for writing a plurality of data bits less than the total number of bits in a data register using a single register write operation (FF 1). The register write circuitry receives data of a single write command (FF 2) wherein the data comprises a bit enable field (FF 5) and a data field (FF 6). For each register write circuit, the bit enable field and the data field have one bit each, which is the same number of bits in each field (FF 2, 5, 6). The register is updated with the bit of the data field that is associated with the enabled bit of the bit enable field (FF 3, 6).

Moreover, Baker teaches all the limitations recited in claim 20 (FF 1-7). Because Baker, taken alone, teaches all limitations of claim 20, we find that the combination of Baker and Runaldue teaches the claimed subject matter. We therefore sustain the Examiner's rejection of claim 20 under 35 U.S.C. § 103(a) as being unpatentable over Baker and Runaldue.

Claim 6

Appellant contends that Baker does not appear to teach that some of the bits of said register are not overwritten (App. Br. 8-9; Reply Br. 14-15).

Baker teaches that some of the bits of the register are not overwritten (FF 1, 3). Because Baker, taken alone, teaches all limitations of claim 6, we find that the combination of Baker and Runaldue teaches the claimed subject matter. We therefore sustain the Examiner's rejection of claim 6 under 35 U.S.C. § 103(a) as being unpatentable over Baker and Runaldue.

Claims 7 and 8

Appellant contends that the combination of Runaldue and Baker does not teach that the data field and the bit enable field are received simultaneously as recited in claim 7 (App. Br. 10-11; Reply Br. 15-16). Appellant also contends that the combination of Runaldue and Baker does not teach that the data field is provided at an address which is contiguous with the address for the bit enable field as recited in claim 8 (App. Br. 10-11).

With respect to claim 7, Baker teaches a data signal 252 that appears on output 270 when the enable 258 is active (FF 5, 6), which means that the data bit and the bit enable bit are both present at the flip-flop at the same time. The claim recitation "data field and the bit enable field are received simultaneously" does not distinguish over this teaching of Baker.

Further, as shown in Baker's Figure 10, the data field (at 252) and bit enable field (at 258) serve as the inputs to the same flip-flop 254. We find that the data field is provided at an address that is contiguous with the address for the bit enable field, as the two inputs are not separated by other data inputs.

Moreover, Appellant has not alleged any reason in support of why placing fields at contiguous addresses would be surprising or unexpected to one skilled in the pertinent art, or why there might have been some unexpected advantage in doing so. Appellant has provided no evidence to show that choosing to address the fields as claimed was "uniquely challenging or difficult for one of ordinary skill in the art." *Leapfrog Enters.,*

Inc. v. Fisher-Price, Inc., 485 F.3d 1157, 1162 (Fed. Cir. 2007) (citing *KSR*, 550 U.S. at 419).

Because Baker, taken alone, teaches all limitations of claims 7 and 8, we find that the combination of Baker and Runaldue teaches the subject matter of the claims. We therefore sustain the Examiner's rejection of claims 7 and 8 under 35 U.S.C. § 103(a) as being unpatentable over Baker and Runaldue.

Claim 10

Appellant contends that the combination of Runaldue and Baker does not teach that the processor subsystem posts an entire command sequence for setting up the data transfer as required by claim 10 (App. Br. 11-12).

The Examiner finds that the PCI-interface ASIC disclosed by Baker is a processor subsystem that posts an entire command sequence for setting up the data transfer (Ans. 22-23). Appellant contends that a person skilled in the art would not consider the PCI-interface of Baker similar to the processor subsystem of claim 10 (Reply Br. 17). However, Appellant has failed to provide any evidence to support this contention. We are not persuaded of error in the Examiner's finding.

We therefore sustain the Examiner's rejection of claim 10 under 35 U.S.C. § 103(a) as being unpatentable over Baker and Runaldue. Claims 9 and 11 fall with claim 10.

Claim 12

Appellant contends that Baker does not teach receiving a data value of a write directed to a control register (App. Br. 12; Reply Br. 5). Appellant contends that the combination of Runaldue and Baker does not teach interpreting bits of the data value as a data field and bits of the data value as an enable field as required by claim 12 (App. Br. 12-14; Reply Br. 5). Appellant also contends that the Examiner has not shown a suggestion or motivation for one skilled in the art to combine the references (App. Br. 14).

We find that Baker teaches receiving a data value of a write directed to a control register (FF 1-3). We also find that Baker interprets bits of the data value as a data field and interprets bits of the data value as an enable field (FF 1, 5, 6). Appellant has provided no definition of the term "interpreting bits" that is contrary to these findings.

We therefore sustain the Examiner's rejection of claim 12 under 35 U.S.C. § 103(a) as being unpatentable over Baker and Runaldue.

Claim 15

Appellant contends that the combination of Runaldue and Baker does not teach a processor subsystem that posts an entire command sequence in the controller for setting up the IDE transfer as recited in claim 15 (App. Br. 15).

Because we conclude that claim 15 is indefinite, we reverse, *pro forma*, the rejection of claim 15. *See In re Steele*, 305 F.2d at 862. We enter a new ground of rejection against the claim, *infra*.

Claim 16

Appellant contends that the combination of Runaldue and Baker does not teach overwriting only bits at bit locations of the register for which a corresponding enable bit in the data value is set with corresponding data bits in the data value (App. Br. 16). To the contrary, Baker teaches overwriting only bits at bit locations of the register for which a corresponding enable bit in the data value is set with corresponding data bits in the data value (FF 1-3).

We therefore sustain the Examiner's rejection of claim 16 under 35 U.S.C. § 103(a) as being unpatentable over Baker and Runaldue.

Claim 22

Appellant contends that the combination of Runaldue and Baker does not teach issuing a write command of the data to the location in memory space for the register (App. Br. 17).

The Examiner finds that Baker teaches issuing write commands at address ranges specified by base address registers of control and status registers (Ans. 23). The claim 22 recitation of "issuing the single write command of the data to the location in memory space for the register" fails to distinguish over this teaching of Baker, and Appellant has provided no evidence or convincing argument to the contrary.

We therefore sustain the Examiner's rejection of claim 22 under 35 U.S.C. § 103(a) as being unpatentable over Baker and Runaldue. Claim 23 falls with claim 22.

New Ground of Rejection -- 37 C.F.R. § 41.50(b)

We reject claim 15 under 35 U.S.C. § 112, second paragraph as being indefinite. Claim 15 depends from independent claim 12. Claim 15 recites "the IDE (integrated drive electronics) data transfer," which lacks proper antecedent basis in the claims.

Appellant may have intended that claim 15 depend from claim 14, which recites "an IDE data transfer" in the first instance. However, we will not speculate on Appellant's intent while the claims are amendable. "[D]uring patent prosecution when claims can be amended, ambiguities should be recognized, scope and breadth of language explored, and clarification imposed." *In re Zletz*, 893 F.2d 319, 321 (Fed. Cir. 1989).

CONCLUSIONS OF LAW

(1) Appellant has failed to show that the Examiner erroneously concluded that the combination of Baker and Runaldue teaches receiving data of a single write command, the data comprising a bit enable field and a data field that comprise N bits in each field, and updating a register with one or more bits of the data field that are associated with enabled bits of the bit enable field.

(2) Claim 15 fails to meet the requirements of 35 U.S.C. § 112, second paragraph.

DECISION

We affirm the Examiner's rejection of claims 2, 3, 5-14, and 16-25 as being unpatentable under 35 U.S.C. § 103(a) over Baker and Runaldue.

We reverse, *pro forma*, the Examiner's rejection of claim 15 as being unpatentable under 35 U.S.C. § 103(a) over Baker and Runaldue.

We have entered a new ground of rejection against claim 15 as being indefinite under 35 U.S.C. § 112, second paragraph.

With respect to the affirmed rejection(s), 37 C.F.R. § 41.52(a)(1) provides that "Appellant may file a single request for rehearing within two months from the date of the original decision of the Board."

In addition to affirming the Examiner's rejection(s) of one or more claims, this decision contains a new ground of rejection pursuant to 37 C.F.R. § 41.50(b). 37 C.F.R. § 41.50(b) provides that "[a] new ground of rejection pursuant to this paragraph shall not be considered final for judicial review."

37 C.F.R. § 41.50(b) also provides that Appellants, WITHIN TWO MONTHS FROM THE DATE OF THE DECISION, must exercise one of the following two options with respect to the new ground of rejection to avoid termination of the appeal as to the rejected claims:

> (1) *Reopen prosecution*. Submit an appropriate amendment of the claims so rejected or new evidence relating to the claims so rejected, or both, and have the matter reconsidered by the examiner, in which event the proceeding will be remanded to the examiner. . . .
>
> (2) *Request rehearing*. Request that the proceeding be reheard under § 41.52 by the Board upon the same record. . . .

Should Appellant elect to prosecute further before the Examiner pursuant to 37 C.F.R. § 41.50(b)(1), in order to preserve the right to seek review under 35 U.S.C. §§ 141 or 145 with respect to the affirmed rejection,

the effective date of the affirmance is deferred until conclusion of the prosecution before the Examiner unless, as a mere incident to the limited prosecution, the affirmed rejection is overcome.

If Appellant elects prosecution before the Examiner and this does not result in allowance of the application, abandonment or a second appeal, this case should be returned to the Board of Patent Appeals and Interferences for final action on the affirmed rejection, including any timely request for rehearing thereof.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a).

AFFIRMED
37 C.F. R. § 41.50(b)

msc

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